



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of

Masaya Kawano

Serial No.: 10/781,904

Group Art Unit: Not Yet Assigned

Filing Date: February 20, 2004

Examiner: Unknown

For: SEMICONDUCTOR DEVICE AND FABRICATION THEREOF

Honorable Commissioner of Patents
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Under the provisions of 37 CFR §1.97 through §1.99 and pursuant to applicant's duty of disclosure under 37 CFR §1.56, applicant respectfully brings the following document listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. A copy of the listed document is provided herewith for the convenience of the Examiner. In compliance with the concise explanation requirement under 37 CFR §1.98(a)(3), the relevance of this document is discussed on page 13 of the subject application. Further, an English-language Abstract is attached to the reference.

This citation does not constitute an admission that the reference is relevant or material to the claims. They are only cited as constituting related art of which the applicant is aware.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-0481.

Respectfully submitted,

Sean M. McGinn, Esq.
Registration No. 34,386

Date:

5/3/04
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INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)

45740/03

Application Number

10/721,904

Applicant(s)

Masaya Kawano

Filing Date

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Group Art Unit

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U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Takehiro Saitoh, et al., "3-Dimensional Elastic-Plastic Finite Element Analysis of Strees-Induced Voiding in Cu Damascene Interconnects of Ultra-Large-Scale Integrated Circuits", Proceedings of Japanese Society for Machine Technology (Division A), Vol. 69,682, June 2003, pp. 964-971 (pp. 4-11).

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.